Parallel (multi-channel, multi-die, multi-LUN) Testing using NanoCycler

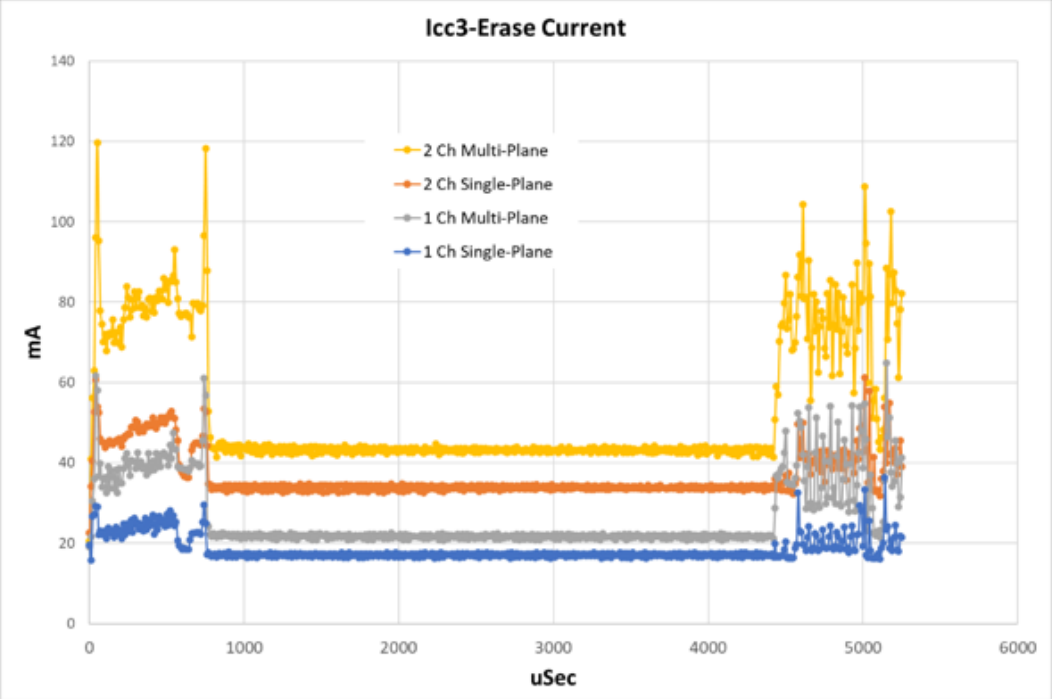
The NAND flash technology (ONFI5) is evolving fast to keep pace with the high-capacity, high-performance high-reliability storage requirements:

- Increased number of dies, LUN, and planes in the same package;
- Increased number of layers;
- I/O speed at and beyond 1.6 GT/sec;
- Shorter program and read times;
- Higher average core and IO currents with extreme peak values.

100+ layers of 3D TLC and QLC NAND devices challenge SSD designers on data, signal, and power integrity.

The knowledge about endurance, retention and disturb sensitivity is crucial to optimize the media management algorithms, paramount for the increased complexity of 3D structures and topologies. A large quantity of statistical data, generated in an application-like environment, is critical to this purpose.

For efficient system-level power integrity solutions, designers need to understand the NAND power profile in the various operation modes. Below, as an example, it is shown the NAND current profile and the effect from the number of planes and active dies.



Overall, the parallel multi-die testing is important to:

- Reduce the test time to collect data from a large set of dies;
- Simulate the behavior of an SSD controller which executes operations with different dies at the same time;
- Extract and optimize the total power consumption profile and minimize spikes and peaks;
- Verify the interference /disturb of operation across different dies;
- Understand and mitigate the thermal implications of the multi-die stack: temperature variation across the stack, thermal analysis, and methods to improve the data reliability;
- Measure the effect of high-speed interface across different NAND channels.
  current profile and the effect from the number of planes and active dies.

Traditional NAND characterization systems show their limitations: characterization at full speed with integrated, real-time power waveform capturing, is required to monitor NAND data, power, and signal integrity at the various operating conditions (temperature, aging, operations' parallelism) to replicate the way NAND works in the SSD or similar target application, to meet product specs, quality, and reliability.

In addition, the effort required to develop the test programs/scripts and to execute them on NAND devices can be very high and consume significant time and resources, if the test and characterization system is basic and not designed to support parallelism and full I/O speed.

The ability to simultaneously execute characterization test programs on several NAND devices, to generate and extract in real-time the massive amount of readout and power data, have been primary objectives for NplusT's new generation of the NanoCycler NAND characterization systems.

NanoCycler HS is a scalable platform for NAND testing and in-depth characterization of performances and reliability.
Unlike competitive systems, NanoCycler performs NAND parallel testing at full I/O speed. The system supports ONFI 5.0 up to 1.6GT/s, with 2.0 GT/s and 2.4GT/s under development for the next NAND generations.

NanoCycler system scalability allows executing simultaneous testing of up to 84 NAND devices per system.
Multiple systems can be cascaded to extend the parallelism beyond 84.

NanoCycler system architecture supports different types of parallel test operations:

- The same test program can be executed on all the Tester Units to have a large DUT population and to gather statistically representative data;
- The same test program can be executed on each Tester Unit with different test parameters (e.g. timing, data patterns,…) or test conditions (temperature, voltage) to identify dependencies, correlations, margins;
- Different test programs can be executed by different Tester Units to reduce total characterization time.

Since each Tester Unit directly connects with a single NAND device, and a NAND device contains up to 16 dies (HDP package), the NanoCyler full system configuration can test up to 1344 NAND dies concurrently.
This results in a system with a total NAND test data bandwidth of about 240 GT/s, assuming NAND I/O speed of 1.6GT/s and 90% of I/O throughput utilization.
Multiple NanoCyler's systems can be cascaded to further increase the total system capacity and data throughput.

Running NAND at full I/O speed is critical to support die parallel operation inside a NAND device.
The table below shows the number of dies that NanoCycler can test in parallel performing NAND read operation, e.g. to extract the NAND Raw Bit Error Rate.

NAND die test parallelism (2 Channels package)

Page size = 16kB tRead = 60uS		# Planes		
		1	2	4
I/O Speed	1,600 MB/s	10	6	2
	2,000 MB/s	14	6	4
	2,400 MB/s	16	8	4

NanoCycler proprietary test controller is based on high-performance FPGA tightly coupled with the NAND device under test. It can control and monitor test conditions (Temperature, Voltage, Power), generate test data patterns, apply back-to-back commands to each die in the package, transfer data, and compute Raw Bit Error Rate data in real-time, at full speed, and with no overhead.

In conclusion, NplusT's NanoCycler performances and capabilities are fully aligned with the NAND technology evolution. It can test and characterize NAND at full speed and parallelism consistently with the conditions of today's actual NAND application. Its proven architecture, hardware, and software scalability enable an unconstrained number of NAND dies to be concurrently and independently tested.