Getting Meaningful Data from NAND Characterization

This article aims to provide a set of hints for engineers working on NAND characterization. The challenge in NAND characterization, essential when building high quality storage systems like SSDs, is in the correct definition of the experiments and in the correct interpretation of the obtained results. Several techniques will be discussed in order to improve the overall characterization process.

1. NEED FOR GOOD CHARACTERIZATION

Modern mass storage systems are using solid state components, mostly NAND flash memories. NANDs are far more cost efficient than components built with other non-volatile memory techniques, so their application is mandatory even if they suffer of inherent failure modes.

The origin of most of the NAND failures is the extremely challenging and fast evolving technology needed to build high density therefore low cost memories. Lower geometry means smaller cells closer to each other which increases the possibility of cell interferences. 3D architecture generates array with different behavior of the cells at every layer. Squeezing multiple bits into the same cell (SLC -> MLC -> TLC -> QLC) reduces the read margin between the different states stored in a single cell, which increases the noise and temperature sensitivity and lowers retention margin. All these issues on top of the "traditional" NAND issues as endurance, retention, self-recovery.

Final products at system level, like SSDs, need to be fast and reliable. As the built-in NAND devices cannot match these requirements, the system controller (SSD controller) has to compensate the NAND failures. Several techniques like ECC, read retry, wear leveling, bad block management, … are used. This is done usually by dedicated algorithms implemented in the controller's firmware.

Writing the efficient algorithms require deep knowledge of the NAND failure modes (what to compensate? how?). Unfortunately, it is not an easy task as every new device or device family has different failure characteristics and these characteristics depend also on the usage mode. Supplier datasheets provide also general reliability information and it is the task of the system developer to find the optimal parameters specific for his/her own application.

This is the reason that NAND characterization at application level is essential. It is worthless to say that only correct definition and execution will provide meaningful results. Otherwise there is the risk that the NAND behavior measured during characterization will be completely different from the performance when these components are built in the storage system.

2. CHARACTERIZATION FLOW

NAND characterization has to be executed in "user mode" as "test mode" is not disclosed by the NAND manufacturers. Test mode would allow higher visibility like the direct measurement of the threshold voltages and currents at cell level, topologic stress, topologic bitmapping … On the other hand, user mode characterization is closer to the final application so the careful definition and execution of a set of experiments can provide meaningful data.

The high level view of a characterization flow is shown in the Figure 1. The characterization shall provide knowledge on the device and on the best LDPC/ECC strategy to be used which brings to the SSD specification and implementation.

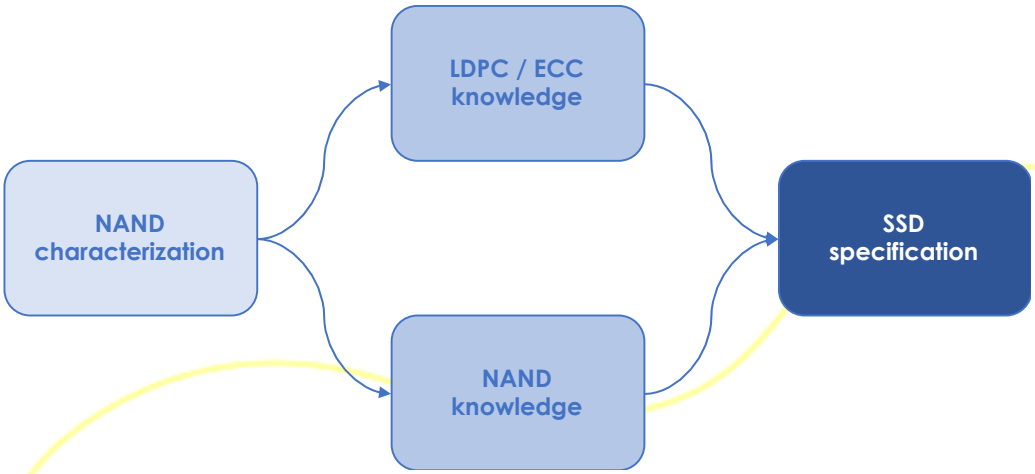

Figure 1: Top Level Characterization Flow

The NAND characterization can be modeled as shown in the Figure 2. The key element is the "experiment". Experiments are executed on a carefully selected set of devices, preconditioned appropriately. Solicitations are applied on these devices and measurements are executed generating a huge quantity of observation data. Data mining techniques are used to extract information from the data, understandable by the human brain, resulting in decisions which can bring the definition of new set of solicitations and pre-conditions.

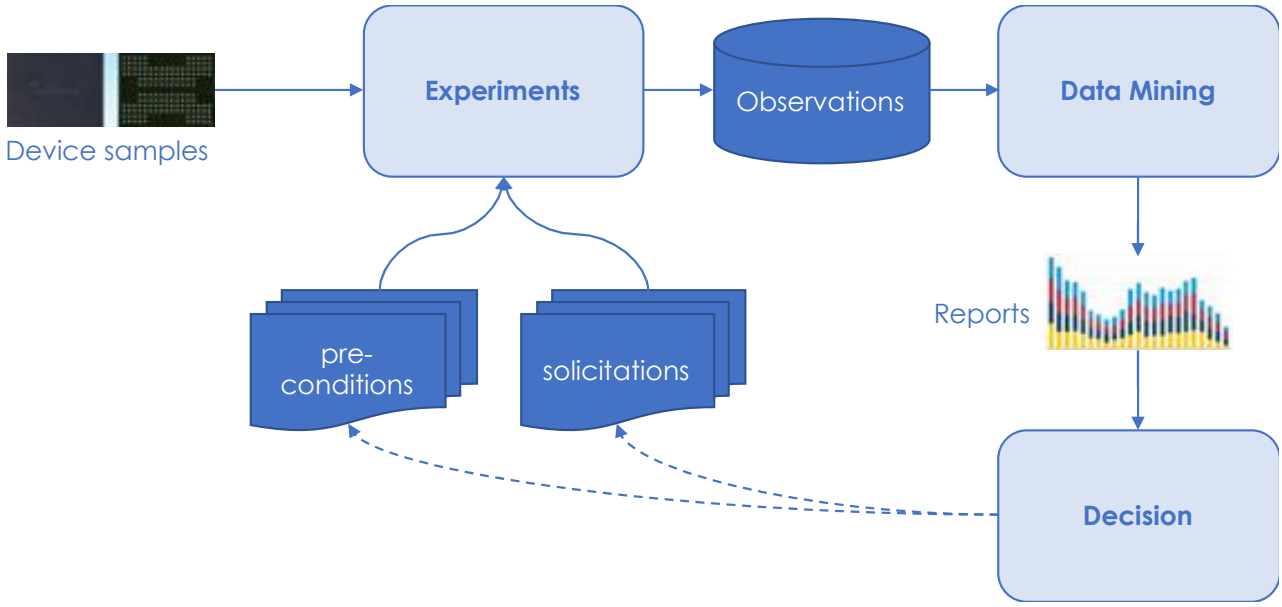

Figure 2 Experiments in the Characterization Flow

3. EXPERIMENT SPECIFICATION

As stated before, experiments are executed in user mode, using the NAND communication interface based on the ONFI standard. Additional elements are temperature, timing and voltages. The Figure 3 provides an overview and the next chapters will describe the details.

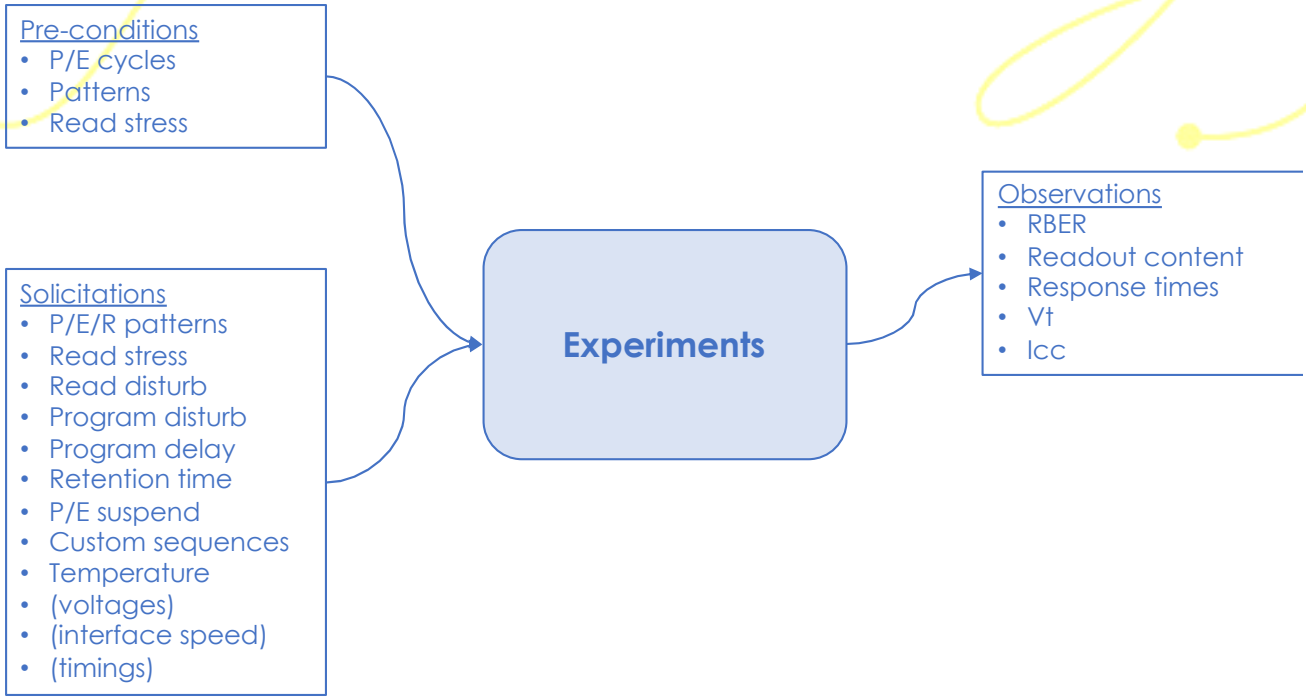

Figure 3 Experiment specification

3.1 Device Samples

Characterization is usually executed on a limited set of samples received from the NAND supplier. These components are often in the engineering sample stadium which increases the probability of device issues.

In order to get reasonable results, the selection is very important and often underestimated.

- The samples have to be built with the same technology (rather obvious) and preferably have to come from the same production lot.
- As experiments run usually on small areas (single block or dozens of blocks) of the large devices, the topologic position of the blocks have to be homogeneous in order to avoid impact of the internal layout on the observation results.
- The topologic position is even more important when working on wordline or on stack layer level.

3.2 Pre-conditions

Pre-conditions bring the devices under tests – or parts of them – into the status where the experiment is executed. Often, the target of the experiment is the same observation with different pre-conditions.

The most commonly used pre-condition is the number of cycles executed on the device before the experiment. As the wear-out effect has a strong impact, the target area has to be accurately preconditioned with program/erase cycles.

The pattern used for program/erase cycling might also have an effect on the results. Pseudo-random or topologic patterns might be applied.

Another, less frequently used pre-condition element is a strong read stress.

3.3 Solicitations

- **P/E/R patterns:** In order to create similar conditions to the final application, usually pseudo-random patterns are used. The quality of the random pattern is essential as the independency of the random patterns on the neighbor blocks. The pattern generation sets a challenge for the test equipment – the calculus speed is important for not impacting the timing of the signal sequences.
- **Read stress:** Application of read commands on the area under stress, to solicit the cells by applying the read voltages. High read number in short time increases the experiment throughput so there is no need to verify the content and even read it out from the page buffers.
- **Read disturb:** Application of the read not on the area to be stressed but on neighbor areas. The performance consideration is the same as for the read stress.

- **Program disturb:** Application of program operations on neighbor areas, usually wordlines. The high voltages needed for programming might influence the state of the disturbed cells.
- **Program delay:** The time between the program operations is crucial to understand dwell effects so it has to be carefully controlled.
- **Retention time:** The time between program and readout. It has to be controlled in order to understand the degradation of the content by time. Also self-recovery phenomena can be detected.
- **P/E suspend:** Suspend operations trigger a combination of several internal phenomena so experiments have to cover this aspect. The timing is crucial as the suspend operation has to be controlled in the specific moment of the operation sequence.
- **Custom sequences:** It might be necessary to experiment of effects of non-standard, supplier specific commands or command sequences.
- **Temperature:** It is a key factor in the reliability. It has a strong impact on the quality of the programming, on the retention and on the disturb/stress sensitivity. Temperature has to be accurately controlled. Certain dice enable the measurement on the on-chip temperature but in general a good package level temperature regulation is suitable.
- **Voltages:** The interface and core voltages might have minor impact on the experiment results.
- **Interface speed:** High speed interface helps to execute experiments fast. On the other hand, the probability of errors due to signal integrity rather than on array problems increase so it has to be designed and validated accurately. Today there are talks about the impact of the interface speed on the array reliability.
- **Signal timings:** It is usually not scope of the experiments.

3.4 Observations

The key of the good quality observation is the separation of the environment inducted problems from the issues the experiments are targeting, coming from the NAND array.

- **RBER:** Raw Bit Error Rate, number of failing bits per block, page or chunk, without any error correction. Like the pattern generation, the high speed calculus is important to reduce experiment overhead and to obtain more accurate timing.
- **Readout content:** In certain experiments, the data reduction to RBER cannot be allowed and the entire bit-per-bit readout content is stored. Obviously this operation causes higher workload for the entire system so it is used only in specific cases.

- **Response times:** Flash operation (erase/program/read) response times provide information about the status of the cells. It is measured on the RDY/BSY signal with adequate (<100nsec) resolution.
- **Vt:** The challenge is to obtain a Vt distribution in user mode, in order to see the shift or the widening of the distributions. Test mode would allow to supply external reference to the cells and successively measure the threshold voltage of every single cell. Limited to user mode, a sufficiently accurate Vt distribution can be obtained using read retry commands.
- **Icc:** Power consumption provides information about the execution of the operation and on the array status. As the accurate dynamic measurement sets a challenge to the test system, its use is rather limited.

4. DATA ANALYSIS

Experiments generate an enormous quantity of data which has to be translated into information. Datalog files are usually stored in database which is the source of the post-processing. As the post-processing algorithms are experiment dependent, their development is part of the experiment.

The outputs are usually 2D or 3D charts, distributions and occasionally topologic or semi-topologic bitmaps.

5. TOOLING

Experiments cannot be executed efficiently without the adequate tooling. The key requirements are the following.

- Execution of several independent experiments in the same time. It means that test programs and test parameters shall be different package per package. As the temperature is part of the test flow and the temperature can change during the experiment, a package level temperature control is essential.
- Tests on different packages should run asynchronously in order to save capacity, mostly for long trials.
- System overhead is also an important factor to keep test times low.
- The tooling has to be well industrialized as system induced errors can cover the real observation results providing meaningless information.
- The management of the experiments has to be straightforward also for not expert users. In order to not to lose flexibility, the best is to have an easy-to-use operator interface and a flexible engineering interface in the same time.
- The data collection has to be automated to avoid risk in the result interpretation.

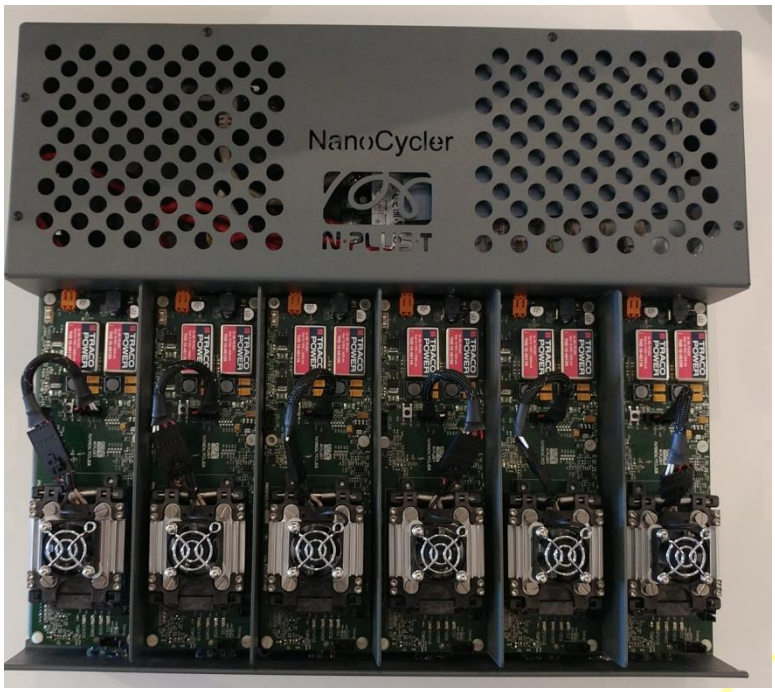

Figure 4 NplusT's NanoCycler NAND characterization equipment

Tamas Kerekes is President and CEO of NplusT, an Italy-based company providing test and characterization equipment and services as well as data analysis software tools for non-volatile memories. Tamas has a strong technical background and expertise in the semiconductor and mass-storage industry. Prior to NplusT, Tamas had several management positions in companies building test and reliability test equipment for the semiconductor and electronics industry. Born in Hungary, he took the degree at the Budapest University of Technology and Economics in 1982.